CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-19 (Canceled).

20. (New) A process for use in the manufacture of application specific integrated circuits comprising the steps of:

providing an in-process semiconductor wafer that lacks a metal one layer and on which has been formed a plurality of circuits that comprise a logic design and at least one programmable circuit;

determining whether modifications to the logic design are desired by examining a completed specimen of the application specific integrated circuits with a metal one layer;

determining desired changes in the metal one layer needed to implement the modifications in logic design, including connecting the at least one programmable circuit to the plurality of circuits; and

forming a metal one layer on said in-process semiconductor wafer different from the metal one layer of the completed specimen to effect the desired changes.

21. (New) The process of claim 20, wherein the act of connecting the at least one programmable circuit comprises interconnecting the plurality of circuits by integrated circuit connection circuitry and connecting the at least one programmable circuit to the integrated circuit connection circuitry.

22. (New) The process of claim 20, further comprising locating at least one configuration register on the in-process semiconductor wafer.

23. (New) The process of claim 22 further comprising storing data for configuration signals in the at least one configuration register.

24. (New) The process of claim 20, wherein the act of providing an in-process semiconductor wafer with at least one programmable circuit comprises providing at least one general purpose logic block that comprises the at least one programmable circuit.

25. (New) The process of claim 20, wherein the act of determining whether modifications to the logic design are desired comprises testing a semiconductor wafer upon which the plurality of circuits have been interconnected by integrated circuit connection circuitry.

26. (New) The process of claim 20, further comprising providing on the in-process semiconductor a configuration register for storing configuration information for the at least one programmable circuit.

27. (New) The process of claim 20, wherein the act of providing an in-process semiconductor wafer with at least one programmable circuit comprises providing a plurality of general purpose logic blocks in a dispersed pattern on the wafer.

28. (New) A process for use in the manufacture of semiconductor device for design changes to be made by metal one level changes, said process comprising the steps of:

providing an in-process semiconductor device having a plurality of standard cells that comprise a logic design when connected by a metal layer and having at least one programmable circuit;

determining whether the logic design should be modified by testing a completed specimen of the semiconductor device with a first metal one layer;

determining changes in the first metal one layer to make a second metal one layer that connects the at least one programmable circuit as part of the logic design; and

forming a metal one layer on said in-process device to make the second metal one layer.